What Is Claimed Is:

1. A method for forming a transistor array on a substrate, comprising the steps of:

forming on the substrate a plurality of signal lines along a first direction and a plurality of gate lines along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel including a first area;

forming a switching unit in the first area of each pixel;

forming a first photoresist layer to cover a first group of the pixels;

forming a second photoresist layer to cover a second group of the pixels; and

forming a third photoresist layer to cover a third group of the pixels,

wherein the first area of each pixel is covered by at least two of the first, second and third photoresist layers.

2. The method of claim 1 wherein the switching units are thin film transistors, and the method further comprises a step of forming a through hole in at least two of the first, second and third photoresist layers within each first area so as to expose each drain electrode of each thin film transistor.

3. The method of claim 2, further comprising a step of forming a conducting layer on the first, second and third photoresist layers, wherein the conducting layer connects to each drain electrode of each thin film transistor via its corresponding through hole.

4. The method of claim 1, further comprising a step of forming a passivation layer between the first photoresist layer and the switching units.

5. The method of claim 4 in which the switching units are thin film transistors, further comprising a step of forming a plurality of through holes in at least two of the first, second, and third photoresist layers and the passivation layer so as to expose drain electrodes of the thin film transistors therein.

6. The method of claim 5, further comprising a step of forming a conducting layer on the first, second and third photoresist layers, and the conducting layer being connected to each drain electrode via each corresponding through hole in the first area.

7. A panel of a flat panel display, comprising:

a glass substrate;

a plurality of signal lines disposed on the glass substrate along a first direction and a plurality of gate lines disposed on the glass substrate along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel including a first area;

a plurality of switching units disposed in the first areas of the pixels;

a first photoresist layer covering a first group of the pixels;

a second photoresist layer covering a second group of the pixels; and

a third photoresist layer covering a third group of the pixels,

wherein the first area of each pixel is covered by at least two of the first, second and third photoresist layers.

8. The panel of claim 7 wherein the switching units are thin film transistors, and, in each first area, the panel further comprises a plurality of through holes in at least two of the first, second and third photoresist layers so as to expose each drain electrode of each thin film transistor therein.

9. The panel of claim 8, further comprising a conducting layer formed on the first, second and third photoresist layers and connected to each drain electrode via each corresponding through hole in the first area.

10. The panel of claim 7, further comprising a passivation layer formed between the first photoresist layer and each switching unit in each first area.

11. The panel of claim 10 wherein the switching units are thin film transistors, and the substrate further comprises a plurality of through holes in at least two of the first, second and third photoresist layers and the passivation layer so as to expose drain electrodes of the thin film transistors.

12. The panel of claim 11, further comprising a conducting layer formed on the first, second and third photoresist layers,

and connected to each drain electrode via each through hole in each first area.

13. A flat panel display, comprising:

a first substrate;

a second substrate facing the first substrate;

a liquid crystal layer disposed between the first substrate and the second substrate;

a plurality of signal lines disposed on the first substrate along a first direction and a plurality of gate lines disposed on the glass substrate along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel having a first area;

a plurality of switching units disposed in the first areas of the pixels;

a first photoresist layer covering a first group of the pixels;

a second photoresist layer covering a second group of the pixels; and

a third photoresist layer covering a third group of the pixels,

wherein the first areas of each pixel is covered by at least two of the first, second and third photoresist layers.

14. The display of claim 13 wherein the switching units are thin film transistors, and the display further comprises a plurality of through holes formed in at least two of the first, second and third photoresist layers so as to expose drain electrodes of the thin film transistors therein.

15. The display of claim 14, further comprising a conducting layer formed on the first, second and third photoresist layers and connected to each drain electrode via its corresponding through hole in the first areas.

16. The display of claim 13, further comprising a passivation layer formed between the first photoresist layer and the switching units.

17. The display of claim 16 wherein the switching units are thin film transistors, and the display further comprises a plurality of through holes formed in at least two of the first, second and third photoresist layers and the passivation layer so as to expose drain electrodes of the thin film transistors therein.

18. The display of claim 17, further comprising a conducting layer formed on the first, second and third photoresist layers and connected to each drain electrode via its corresponding through hole.